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Introduction
Device tree basics
Walking through a DTS file
Defining a peripheral
Summary

A sample device tree .dts listing (cont.)

```
ps7_axi_interconnect_0: axi@0 {
    #address-cells = <1>;
    #size-cells = <1>;
    compatible = "xlnx,ps7-axi-interconnect-1.00.a", "simple-bus";
    ranges ;
    gic: interrupt-controller@f8f01000 {
        #interrupt-cells = < 3 >;
        compatible = "arm,cortex-a9-gic";
        interrupt-controller ;
        reg = < 0xf8f01000 0x1000 >,< 0xf8f00100 0x100 >;
    } ;
    pl310: pl310-controller@f8f02000 {
        arm,data-latency = < 3 2 2 >;
        arm,tag-latency = < 2 2 2 >;
        cache-level = < 2 >;
        cache-unified ;
        compatible = "arm,pl310-cache";
        interrupts = < 0 34 4 >;
        reg = < 0xf8f02000 0x1000 >;
    } ;

    [ ... more peripheral definitions ... ]
};
```

Eli Billauer

The Device Tree: Plug and play for Embedded Linux

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PrimeCell Level 2 Cache Controller (PL310) Technical Reference Manual.. L2 Cache Controller, PL310 (ADSP-SC58x Only) ... 106.7k words of 48-bit instructions (or 40-bit data), or combi- ... A download link for a specific BSP is.. controlled CPU instructions from accessing a cache par- ... memory is mapped to the CPU caches, these defenses ... PL310 Cache Controller Technical.. Readme imx6 linux - Free download as PDF File (. ... Our current configuration does not configure the PL310 L2 cache controller and does not set the ACTLR.. Supports dispatch of 4 instructions and completion of 7 instruction per clock ... PL310. L2 Cache. Controller. IRQ/FIQ. PL390. Interrupt. Controller. Cortex A9.. Zynq-7000 SoC Technical Reference Manual ... 3.4.5 Enabling and Disabling the L2 Cache Controller. ... The L2 cache controller is based on the ARM PL310 and includes an 8-way ... mode to download test software. 0x2111.. case 6: /*. * PXA 3XX. *. * See <http://download.intel.com/design/intelxscale/31628302.pdf>. */ ... PrimeCell Level 2 Cache Controller (PL310). * The addition of an PI310 Cache Controller Pdf Download. This preface introduces the PL310 Cache Controller Revision r0p0 Technical Reference Manual. It contains the following user guide can be downloaded from <http://www.ti.com/lit/zip/SPRU656>. How to Use this Manual. Novice users unfamiliar with memory caches should read this Keywords encrypted memory, encrypted RAM, AES, cold boot, bus monitoring, DMA ... sets the PL310 L2 cache controller and zeros the L2 cache contents. As a result, sensitive data ... futureplus.com/download/datasheet/fs2334_ds.pdf, 2006.. The L2 Cache Controller (L2CC) is based on the L2CC-PL310 ARM multiway ... downloading code and single-stepping through the program.. This makes them susceptible to an inexpensive class of memory attacks, such as cold-boot ... PL310 cache controller reference manual, 2007.. cache have been (at least partially) replaced by the instructions and data of τb . Thus ... [2] ARM, PL310 Cache Controller Technical Reference Manual, 2007.. PL310 Cache Controller Revision: r0p0 Technical Reference Manual Copyright 2007 ARM Limited. All rights reserved. ... Save, download, print and share.

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